REMARKS

Claims 2, 4-7, 9, 11-13, 15, 17, 19-22, 24, 26, 27, 29-36, and 38-43 are pending in the present application.

In the office action mailed December 24, 2003 (the "Office Action"), claims 9, 2, 3, 5, 6, 17, 18, and 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,953,015 to Choi (the "Choi patent"). Claims 4, 15, 11-14, and 19-22 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent in view of National Semiconductor, "Easy Logarithms for COP400" (the "NS reference"). Claims 26-28, 30, 32-37, and 39-43 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent in view of U.S. Patent No. 6,292,191 to Vaswani et al. (the "Vaswani patent"). Claims 29 and 38 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent in view of the Vaswani patent and further in view of the NS reference.

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

As previously mentioned, claims 9, 2, 3, 5, 6, 17, 18, and 24 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent. The Examiner cited common knowledge in the art of "dividing by two after approximating a base-two logarithm of the square of the ratio and to have the integer portion five bits in length." *See* the Office Action at page 2, paragraph 2a. Consequently, the Examiner argues, that claim 9 would have been unpatentable over the combination of the Choi patent and the common knowledge.

Claims 9 and 24 are patentable over the Choi patent in view of the common knowledge in the art, as characterized by the Examiner, because the combination thereof fails to teach or suggest the combination of limitations recited by claims 9 and 24, and the common knowledge in the art cited by the Examiner fails to make up for the deficiencies of the Choi patent. The Choi patent describes a circuit and method for determining the level-of-detail (the "LOD") for texture mapping in computer graphics. As described in the Choi patent, the circuit includes a look-up table ("LUT") 210 storing precalculated values of a simplified function for a

LOD calculation to provide faster and simpler computation of the LOD. *See* Figure 2 and col. 3, lines 49-54. In calculating a LOD, the gradients between texels of a texture map and pixels of a display coordinate system are provided to multiplexers 220 and 224. Each of the multiplexers 220 and 224 select the gradients for an axis of the texture map related to a common axis of the display coordinate system. The values are provided to a pre-processor 240 which uses the selected gradients to calculate indices. The LUT 210 is accessed by using the indices to select which of the precalculated values are to be processed by a post-processor 250. *See* col. 3, lines 55-63. The post-processor 250 calculates partial LOD ("LODP") values which are stored in registers 260 and 262. A comparator 270 determines the maximum of the two LODP values stored in the registers 260 and 262 and outputs the greater of the two as the LOD. *See* col. 4, lines 2-14.

In precalculating the values of the simplified function for storage in the LUT 210, only the values for a limited range of gradients is provided. In the event that the gradient is beyond the limited range of values stored in the LUT 210, the gradient value is scaled accordingly to select values stored in the LUT 210. *See* col. 4, lines 15-38. The post-processor 250 adjusts the LODP values in the event scaling is necessary before they are stored in the registers 260 and 262. *See* col. 4, lines 39-44.

In contrast to the circuit and method described in the Choi patent, claim 9 recites a method for computing a level-of detail (LOD) for the application of texels of a texture map to pixels of a graphics image where the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis are calculated, and the greater to the *squares of the first and second ratios* are selected for computing the LOD. Claim 24 similarly recites an apparatus adapted to receive signals representing texel coordinates for texels of a texture map and pixel coordinates for pixels of a graphics image to calculate a LOD, the apparatus calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis, selecting the greater of the *square of the first ratio and the square of the second ratio*, and approximating a base-two logarithm *of the selected square of the ratio.*

As previously discussed, the system and method described by the Choi patent generates two partial LOD values from the precalculated value selected from the LUT 210 based on the first and second gradients. The system and method described in the Choi patent does not select from the greater of the first and second gradients provided to the pre-processor 240. The LODP for one axis is stored in the register 260 and the LODP for a second axis is stored in the register 262. The final LOD value is selected from the two LODP values by the comparator 270. In contrast to claims 9 and 24, the circuit and method disclosed in the Choi patent does not select the greater of the two gradients along respective axes to calculate the LOD, but instead uses all the gradients du/dx, dv/dx and du/dy, dv/dy from each axis of the display coordinate system, x and y, to calculate respective LODP values stored in two separate registers 260 and 262. *See* col. 3, line 61-col. 4, line 14. The greater of the two LODP values is selected and provided as the LOD calculated by the circuit and method.

Moreover, attempting to modify the Choi patent in order to make up for the deficiencies previously described would render the circuit unsuitable for its intended purpose. As described in the Choi patent, "computation is made faster and simpler by providing a lookup table (LUT)." Col. 3, lines 49-51. The use of the LUT as described in the Choi patent cannot be implemented if particular gradients between the texture map and the display coordinate space are selected based on which value is greater. The indices are calculated based on both the gradients for each of the display axes. Thus, selecting the greater of the first and second ratios between the number of texels for one pixel along first and second axes, respectively, cannot be accommodated by the circuit and method disclosed in the Choi patent.

Thus, even if it assumed that the Examiner's characterization of the common knowledge is accurate, that is, it is well known in the art to divide by two and have the integer portion five bits in length, the common knowledge does not make up for the deficiencies of the Choi patent previously discussed. The common knowledge as described by the Examiner does not change the manner in which the LOD is calculated as described in the Choi patent. Regardless of the division by two, or the five bit integer portion, the calculated LOD is still selected from two partial LODs that are calculated for each axis of the display coordinate space. That is, the use of an LUT 210 for storing precalculated values that are selected by indices resulting from the gradient values between a texture map and a display coordinate space does not

change if the circuit and method of the Choi patent is modified by what has been characterized by the Examiner as common knowledge.

For the foregoing reasons, claims 9 and 24 are patentable over the Choi patent and the common knowledge, as characterized by the Examiner. Claims 2, 5, and 6, which depend from claim 9, and claim 17, which depends from claim 24, are similarly patentable over the Choi patent based on their dependency from allowable base claim 9. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. However, because each claim in an application represents an invention of different scope, the rejection of an independent claim does not necessarily result in the rejection of the claims depending therefrom. Claims 3 and 18 have been cancelled by amendment. Therefore, the rejection of claim, 2, 5, 6, 9, and 17 under 35 U.S.C. 103(a) should be withdrawn.

As previously mentioned, claims 4, 15, 11-14, and 19-22 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent in further view of the NS reference. Claim 15 is patentable over the Choi patent in view of the NS reference because the combined teachings of the Choi and NS references fail to teach or suggest the combination of limitations recited by claim 15.

Claim 15 recites, in pertinent part, a method for computing a LOD for application of texels of a texture map to pixels of a graphics image, the method comprising calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis, and selecting the greater of the square of the first ratio and the square of the second ratio for calculating the LOD. As previously discussed with respect to claims 9 and 24, the Choi patent does not disclose selecting the greater of the square of the first ratio and the square of the second ratio for calculating the LOD. The circuit and method described in the Choi patent uses the gradients of each axis of the display coordinate space to calculate two different partial LODs. The gradients are used, in particular, to generate indices to access an LUT storing precalculated values of a simplified formula for calculating LODT values, which are then used to calculate two LODPs. One of the two partial LODs is selected based on the greater of the two values, and is provided as the final LOD. Claim 15, in contrast, selects the greater of the square of first and

second ratios, and uses the selected square of the ratio for calculating the LOD. Selection is not between two partial LODs, as in the Choi patent.

The NS reference, which has been cited by the Examiner as teaching "shifting the square of a number left by the number of leading zeros and the MSB, effectively ignoring the MSB; calculating a characteristic (integer) based on the number of characteristic bits minus the number of shifts required, effectively the [(number of integer bits - 1) - LZs]; concatenating the integer value to first number; and defining the resulting number as the integer portion." *See* the Office Action at page 5, paragraph 3a (citations omitted). Even if it is assumed that the Examiner's characterization of the NS reference is accurate, it does not make up for the deficiencies of the Choi patent, as previously discussed. The teachings as characterized by the Examiner do not change the manner in which the Choi patent calculates LOD, which as previously discussed, does not select the greater of the squares of a first and second ratio.

Moreover, one ordinarily skilled in the art would not have been motivated to combine the teachings of the Choi patent and the NS reference because the Choi patent does not contemplate performing a logarithmic calculation through an approximation, but uses an LUT storing precalculated values to simplify the calculation of the LOD. That is, the circuit and method described in the Choi patent does not approximate the logarithmic calculation for each of the input gradient values, but instead, selects from a limited number of precalculated values as part of calculating an LOD. The computations performed in the Choi patent is for calculating indices to access the precalculated values stored in the LUT, which result from logarithmic calculations. Additional computations may be performed for adjusting the LODP values where scaling has occurred. As described at col. 5, line 32-col. 6, line 16, the computations by the pre- and post-processors 240, 250 are not directed to logarithmic calculations, but are directed to merely generating an index number and adding the selected precalculated value with a constant k, related to scaling.

For the foregoing reasons, claim 15 is patentable over the Choi patent in view of the NS reference. Claims 11-13, which depend from claim 15, are similarly patentable based on their dependency from allowable claim 15. Claim 4 is patentably based on its dependency from allowable claim 9. Therefore, the rejection of claims 4, 11-13, and 15 under 35 U.S.C. 103(a) should be withdrawn.

As previously mentioned, claims 26-28, 30, 32-37, and 39-43 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent in view of the Vaswani patent.

Claims 26 and 35 are patentable over the Choi patent in view of the Vaswani patent because the cited references, alone or in combination, fail to disclose or suggest the combination of limitations recited by claims 26 and 35. Claim 26 recites a graphics processing system including, among other things, a LOD computation circuit similar to the apparatus of claim 24. Claim 35 recites a computer system having a LOD computation circuit similar to the apparatus of claim 24. As previously discussed with respect to claims 9, 24, and 15, the Choi patent does not disclose selecting the greater of the squares of first and second ratios for calculating the LOD. The Vaswani patent has been cited by the Examiner for teaching "a bus interface for coupling to a system bus; a graphics processor coupled to the bus interface to process graphics data; address and data busses coupled to the graphics processor to transfer address and graphics data to and from the graphics processor; display logic coupled to data bus to drive a display." *See* the Office Action at page 9, paragraph 4a (citations omitted). Even if it is assumed that the Examiner's characterization of the Vaswani patent is accurate, its teachings fail to make up for the deficiencies of the Choi patent previously discussed with respect to claims 9, 15, and 24.

For the foregoing reasons, claims 26 and 35 are patentable over the Choi patent in view of the Vaswani patent. Claims 27, 30, 32-34, which depend from claim 26, and claims 36 and 39-43, which depend from claim 35, are also patentable based on their dependency from a respective allowable base claim. Claims 28 and 37 have been cancelled. Therefore, the rejection of claims 26, 27, 30, 32-36, and 39-43 under 35 U.S.C. 103(a) should be withdrawn.

Claims 29 and 38 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Choi patent in view of the Vaswani patent, and further in view of the NS reference. Claim 29 depends from allowable claim 26, and claim 38 depends from allowable claim 35. Consequently, claims 29 and 38 are patentable based on their dependency from a respective allowable base claim, and therefore, the rejection of claims 29 and 38 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP

Kimton N. Eng
Registration No. 43,605
Telephone No. (206) 903-8778

KNE:ajs

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DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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